# The New Method for Sigma-Delta Converter Signal Evaluation

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*Abstract* - **A sigma-delta converter consists of a sigma-delta modulator that is essentially a high speed, low resolution anlog-digital converter (ADC), and a digital signal processing stage that trades time for resolution and filters the output of the modulator. In this paper, the New Synchronous Voltage to Frequency Converter (NSVFC) based on "sigma delta" (Σ-Δ) ADC is described. This converter with additional logic works similarly as conventional ADC but it has a better frequency spectral property then other Σ-Δ ADC and therefore it is possible to use this converter for output signal evaluating based on phase locked loop (PLL). A experimental NSVFC was constructed and simulated (MATLAB) to verify operation of the converter. Analysis and prototype of NSVFC is also described.**

## I. INTRODUCTION

The voltage to frequency converter (VFC) has become quite popular due to their low cost and application versatility in variety of electronic control and measurement systems. With a good quality VFC, this circuit will match the performance of many commercial A/D converters. Its only disadvantage is relatively long conversion time. Σ-Δ ADC [1] can be used for synchronous VFC (SVFC). In SVFC charge balance pulse length is now defined by two successive edges of the external clock. The block diagram of the Σ-Δ VFC is shown on Fig. 1. If this clock has low jitter the charge will be defined very accurately. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and they have excellent temperature stability [2], but is not pure tone for constant input voltage (output pulses are not equally spaced). Fig. 2 c) shows the waveforms of Σ-Δ SVFC. From Fig. 2 c) can be seen that output periods are not the same, but they have changed between 3 and 4 clock cycles. This disadvantage was taken away in NSVFC1 and NSVFC2.

## II. NEW SYNCHRONOUS VFC

In Fig. 3 is NSVFC1 block diagram. Only one-shot is added and connected to comparator output. Fig. 2 shows waveforms of this NSVFC1. Number of pulses is same for usual Σ-Δ SVFC [2] and NSVFC (NSVFC1 and NSVFC2). The output frequency $f_O$ is given by (1):

$$f_O = f_{CLK} (1 - V_i / V_R) / 2 \qquad [\text{Hz, V}] \qquad (1)$$

where $V_i$ is input voltage, $V_R$ is reference voltage and $f_{CLK}$ is clock frequency. It is important to note, that for NSVFC1 this equation is limited for $V_{imin}$ given by (2). The minimal input voltage value $V_{imin}$ (for NSVFC1):

$$V_{imin} > 2 f_{CLK} V_R t_{dC} \qquad [\text{V, Hz, sec}] \qquad (2)$$

where $t_{dC}$ is comparator time delay. E.g. for $f_{CLK} = 10$ *kHz*, $V_R = 5$ *V* and $t_{dC} = 200$ *ns*, the minimal value $V_{imin} > 0.02$ *V*.

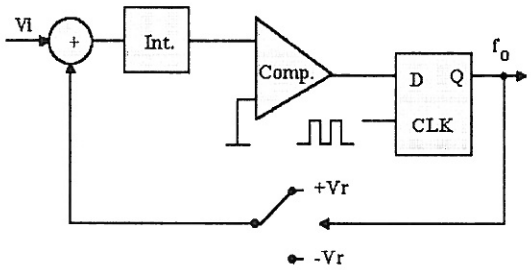


Figure 1. Conventional Σ-Δ ADC used as voltage to frequency converter (SVFC). Int. - integrator, Comp. - comparator, $V_i$ - input voltage, $V_R$ - reference voltage, D - flip flop.

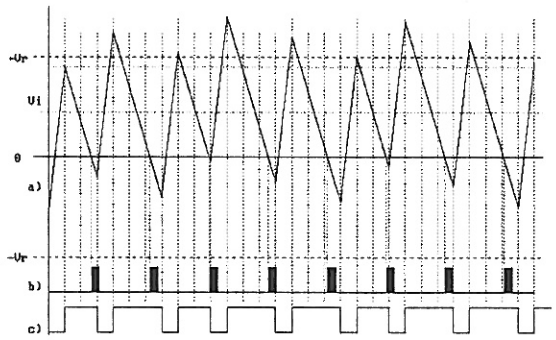


Figure 2. Waveforms of SVFC (a, c) and NSVFC (a, b, c). a) integrator - output voltage, b) one shot output, c) D-flip flop output. $V_i = 1.8$ V, $V_R = 4$ V, period of one shot is $3.636\ T_{clk}$

## III. NSVFC OUTPUT FREQUENCY EVALUATION

The key to Σ-Δ modulator is the integrator. At each conversion, the integrator keeps a running total of its previous output and its current input. The output from the integrator is feed to 1-bit analog/digital converter (ADC). This is simply a comparator with its reference input at a level of half the input range, 0 V in this case. The ADC output feeds a 1-bit digital/analog converter (DAC) which has output levels equal $+V_R$ or $-V_R$. A summing amplifier completes the loop by summing the current input signal and the previous sample DAC output. The aim of the feedback loop is to try to maintain the average output change of the integrator at the comparator reference level, 0 V. Therefore:

$$const + \sum_{k=1}^{\infty} V_{o1}(k) + \sum_{k=1}^{\infty} V_{o2}(k) = 0 \qquad (3)$$

where $k = 1, 2, \ldots \infty$, *const* is voltage depending on starting conditions and $V_{o1}(k)$ and $V_{o2}(k)$ are integrator output voltage in $k$ output frequency period, see Fig. 4. The NSVFC and equivalent period time diagram is shown on Fig. 5.

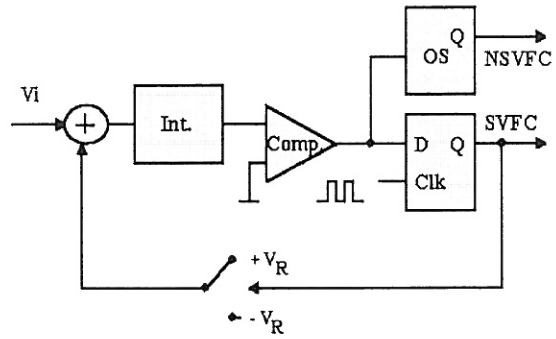


Figure 3. NSVFC1 - New Σ-Δ voltage to frequency converter type1. Int. - integrator, Comp. - comparator, $V_i$ - input voltage, $V_R$ - reference voltage, D - flip flop, OS - one shot.

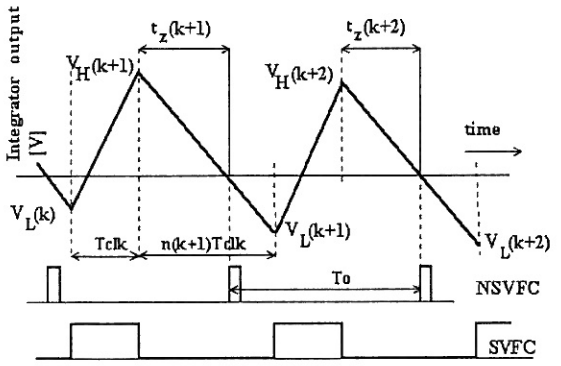


Figure 4. Time diagram for ideal converter - output frequency evaluation

Change $\Delta V_a$ is given by (4):

$$\Delta V_a = C \int_0^{T_{clk}} (V_i(t) + V_R)dt \qquad (4)$$

and $\Delta V_b$ is given by (5):

$$\Delta V_b = C \int_0^{nT_{clk}} (V_i(t) - V_R)dt \qquad (5)$$

where C is the integrator constant. The integrator output is given by:

$$V_{o1}(k) = V_{o2}(k-1) + C \int_0^{T_{clk}} (V_i(t) + V_R)dt \qquad (6)$$

$$V_{o2}(k) = V_{o1}(k) + C \int_{T_{clk}}^{(n+1)T_{clk}} (V_i(t) - V_R)dt \qquad (7)$$

and for $V_i(t) = V_i$ (constant input voltage):

$$V_{o1}(k) = V_{o2}(k-1) + C(V_i + V_R)T_{clk} \qquad (8)$$

$$V_{o2}(k) = V_{o1}(k) + C(V_i - V_R)nT_{clk} \qquad (9)$$

Integrator output voltage change is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)nT_{clk} \qquad (10)$$

where $n$ must be an integer for SVFC. For NSVFC output is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)mT_{clk} \qquad (11)$$

where $m$ is real for NSVFC. From (11) $(V_R > V_i)$:

$$m = \frac{V_i + V_R}{V_R - V_i} \qquad (12)$$

and for SVFC, $n$ is given by (13):

$$n = ceil\left(\frac{V_i + V_R}{V_R - V_i}\right) = ceil(m) \qquad (13)$$

where Ceil(.) - Converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. Ceil(9/3)=3, Ceil(9.01/3) =4.

## IV. OUTPUT FREQUENCY EVALUATION FOR IDEAL NSVFC

For this ideal NSVFC it is supposed, that comparator has a zero time delay and noise value voltage on second comparator input is zero. Output period for NSVFC can be determined from Fig. 4. It is supposed, that $V_R > V_i$, where $V_R$ is reference voltage and $V_i$ is input voltage. The $V_L(i)$ and $V_H(i)$ are voltage at integrator output.
Output period $T_0$ from Fig. 6 is given by:

$$T_0 = T_{clk}[n(k+1) - t_z(k+1) + 1 + t_z(k+2)] \qquad (14)$$

Time from $V_L(i)$ to $V_H(i+1)$ is always $1*T_{clk}$ if no error occurs (error can be caused by comparator delay, comparator hysteresis or voltage change on second comparator input. This will discuss in next part). For $T_{clk} = 1$, the output period ${}^1T_0$:

$${}^1T_0 = n(k+1) - t_z(k+1) + 1 + t_z(k+2) \qquad (15)$$

Strait line from $V_L(i)$ to $V_H(i+1)$ has a slope: $V_i + V_R$
The line is given by equation (all following equations are given for $T_{clk} = 1$):

$$V_H(k+1) = V_L(k) + (V_i + V_R).1 \qquad (16)$$

The line slope from $V_H(i)$ to $V_L(i+1)$ is: $V_R - V_i$. Line equation is:

$$V_L(k+1) = V_H(k+1) - (V_R - V_i)\, n(k+1) \qquad (17)$$

where $n(k+1)$ is given by:

$$n(k+1) = ceil(V_H(k+1)/(V_R - V_i)) = ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \qquad (18)$$

hence

$$V_L(k+1) = V_H(k+1) - (V_R - V_i)\, n(k+1) = V_H(k+1) - (V_R - V_i)\, ceil(V_H(k+1)/(V_R - V_i)) = V_L(k) + V_i + V_R - (V_R - V_i)\, ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \qquad (19)$$

The term $(V_R - V_i)\, ceil((V_L(k) + V_R + V_i)/(V_R - V_i))$ can't be reduced, because *ceil()* is nonlinear function, e.g.: $y(ceil(x/y)) \neq ceil(x)$.
Time $t_z(k)$ is given by:

$$t_z(k) = V_H(k)/(V_R - V_i) \qquad (20)$$

Output period equation is given by (for $T_{clk} = 1$):

$$^{1}T_0 = n(k+1) - t_z(k+1) + 1 + t_z(k+2) =$$
$$ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) - V_H(k+1)/(V_R - V_i)$$
$$+ 1 + V_H(k+2)/(V_R - V_i) \quad (21)$$

After multiplication by term $(V_R - V_i)$, equation (21) is changed to:

$$(V_R - V_i)^{1}T_0 = (V_R - V_i)\, ceil((V_L(k) + V_R + V_i)/(V_R - V_i))$$
$$- (V_L(k) + V_R + V_i) + V_R - V_i + V_L(k+1) + V_R + V_i \quad (22)$$

$V_L(k+1)$ is substitute by equation (19), hence:

$$(V_R - V_i)^{1}T_0 = (V_R - V_i)ceil((V_L(k) + V_R + V_i)/(V_R - V_i))$$
$$-(V_L(k) + V_R + V_i) + 2V_R + V_L(k) + V_i + V_R - (V_R - V_i)$$
$$ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \quad (23)$$

After reduction, output period $^{1}T_0$ is given by:

$$^{1}T_0 = 2V_R/(V_R - V_i) \quad (24)$$

and output frequency $^{1}f_0$ hence:

$$^{1}f_0 = (V_R - V_i)/2V_R \quad (25)$$

and for $T_{clk} \neq 1$ the output frequency $f_0$:

$$f_0 = f_{clk}\,(V_R - V_i)/2V_R \quad (26)$$

where $f_{clk} = 1/T_{clk}$

From (26) is shown, that ideal NSVFC output frequency is linearly dependent on input voltage ($f_{clk}$ and $V_R$ are constants).

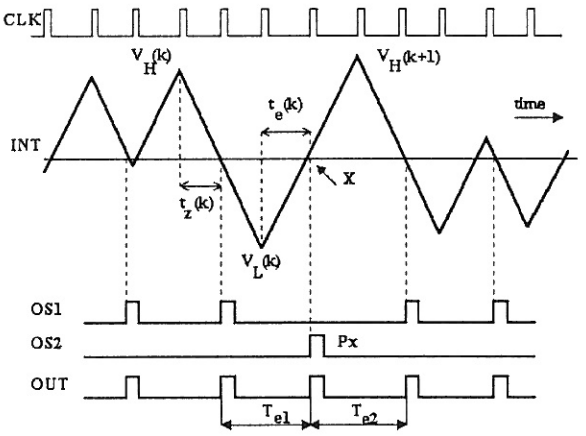


Figure 5. Time diagram for real converter - output frequency evaluation

## V. OUTPUT FREQUENCY EVALUATION FOR REAL NSVFC

In this part, error caused by comparator delay, comparator hysteresis or voltage change on second comparator input is described. This error is displayed on Fig. 5 and is sign by X point. The error can arise especially when input voltage $V_i \approx 0$. The error occur when 2 clock cycles are need for $V_L(k)$ to $V_H(k+1)$ transition. In this case, this error must be detected and additional output pulse generated. When integrator output voltage on one comparator input is greater than voltage on second comparator input (it is important to note, that in ideal condition, output pulse is generated only when voltage on integrator output is lower then voltage on second comparator input - leading edge of integrator output). The additional logic is used for this purpose. The block diagram of this NSVFC2 is shown in Fig. 6. Output period $T_0$ from Fig. 5 is given by:

$$T_{e1} = T_{clk}\,[n(k) - t_z(k) + t_e(k)] \quad (27)$$

For $T_{clk} = 1$, $V_i << V_R$ output period $^{1}T_{e1}$ is given by:

$$^{1}T_{e1} = ceil(V_H(k)/(V_R - V_i)) - V_H(k)/(V_R - V_i)$$
$$+ |V_L(k)/(V_R + V_i)| \quad (28)$$

In (28) $ceil(V_H(k)/(V_R - V_i)) = 2$ and $V_H(k) \approx V_R$ and $|V_L(k)| \approx V_R$ for $V_i \approx 0$. Hence:

$$^{1}T_{e1} = 2 - V_R/(V_R - V_i) + V_R/(V_R + V_i) \approx 2(1 - V_i/V_R) \quad (29)$$

Similarly the output period $^{1}T_{e2}$ is given by:

$$^{1}T_{e2} = 2 - t_e(k) + V_R/(V_R - V_i)$$
$$= 2 - V_R/(V_R + V_i) + V_R/(V_R + V_i) \approx 2(1 + V_i/V_R) \quad (30)$$

Equations (29) and (30) for $T_{clk}$ are simplified to:

$$T_{e1} \approx 2T_{clk}\,(1 - V_i/V_R) \quad (31)$$

$$T_{e2} \approx 2T_{clk}\,(1 + V_i/V_R) \quad (32)$$

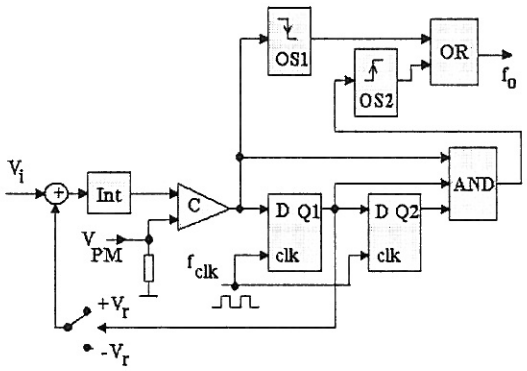


Figure 6. NSVFC2 - Block diagram. Int. - integrator, C - comparator, $V_i$ - input voltage, $V_r$ - reference voltage, $V_{PM}$ - input voltage for phase modulation, D - flip-flop, OS - one shot, AND, OR - log. function.

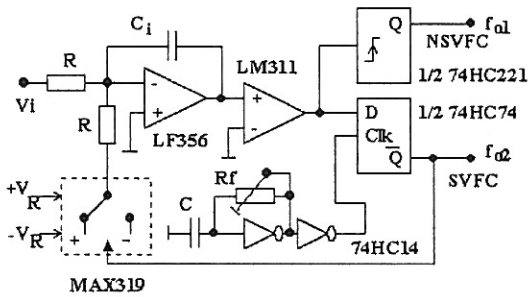


Figure 7. Experimental NSVFC1 simplified circuit diagram.

## VI. V/F EXPERIMENTAL RESULTS

Commercially produced SVFC AD7741 and AD7742 [2] were tested and also NSVFC1 was realized and tested [12], [13], [14], [15]. In Fig. 7, experimentally realized NSVFC1 simplified circuit diagram is shown [3]. The voltage/frequency characteristic and frequency spectrum was measured. In common type of SVFC, since the output pulses are synchronized to a clock they are not equally spaced. This need not affect the user of a SVFC for A/D conversion [16], [17], but it does prevent its use as a precision oscillator. Despite this

disadvantage the improvement in performance makes the SVFC ideal for the majority of high-resolution VFC applications. In Fig. 8, the frequency spectrum of SVFC is shown and in Fig. 9, the spectrum of NSVFC1 is displayed. From Fig. 9 can be seen, that spurious spectral lines are rejected.

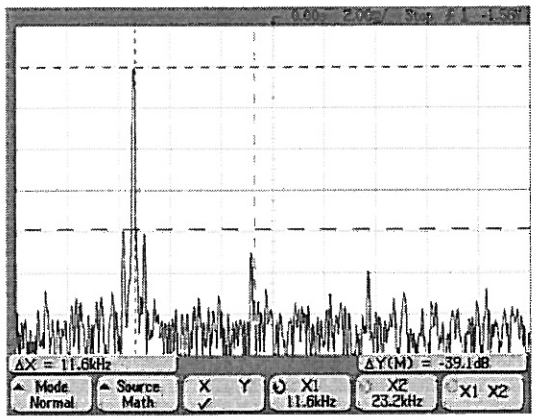


Figure 8. The frequency spectrum of traditional Σ-Δ V/f converter

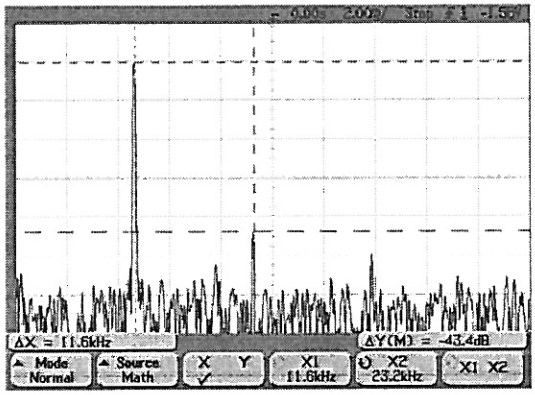


Figure 9. The frequency spectrum of new, modified Σ-Δ V/f converter (NSVFC1).

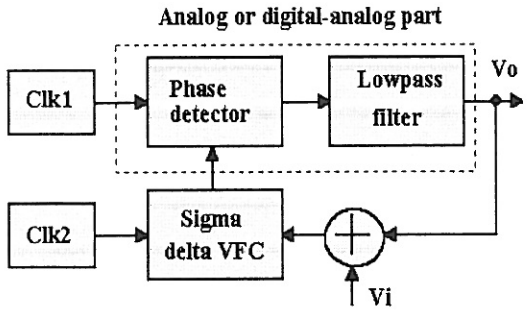


Figure 10. Block diagram of phase locked loop system with Σ-Δ V/f converter.

## VII. COMPENSATING VOLTAGE MEASUREMENT BASED ON PLL

The block diagram of PLL compensating voltage measuring system with Σ-Δ V/f converter is shown in Fig. 10. Phase detector and Lowpass-filter can be analog or digital. The system (output voltage) has also smoothing possibility. Block diagram MATLAB simulated system is shown in Fig. 11.

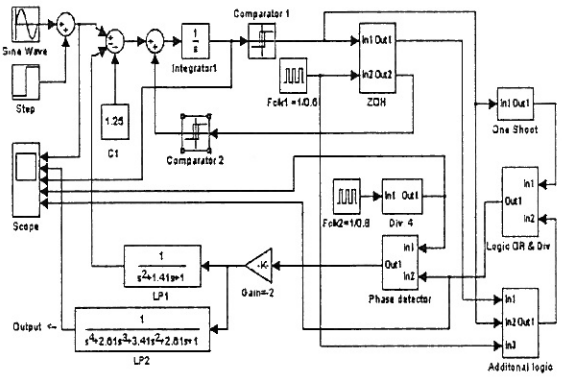


Figure 11. Block diagram of simulated PLL system

The input analog signal, output analog signal, integrator output and clock pulses for input step voltage and step voltage + sin(.) are shown in Fig. 12 and 13.

## VIII. CONCLUSION

A very detailed look at the concept of new type sigma-delta voltage to frequency converter circuit has been presented in this article. A prototype system was constructed to verify operation of the converter. Analysis of new type voltage to frequency converter was described. The NSVFC simulation results and measured results were compared. From analysis, simulation and measured results can be seen very good agreement from different points of view. It was pointed out that this new converter has better properties than other synchronous types of VFC and can be used for compensating voltage measurement.


## ACKNOWLEDGMENT

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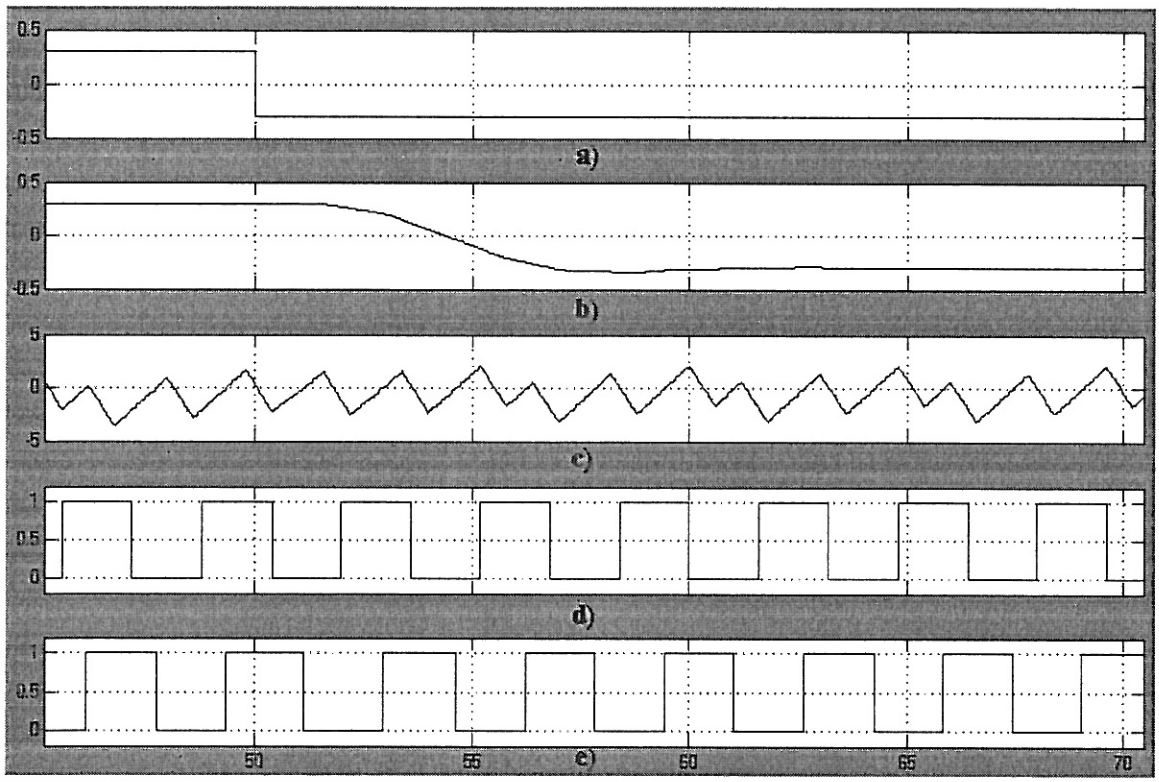


Figure 12. Time diagrams of: a) input voltage, b) output voltage, c) integrator output, d) Clk1clock, e) Σ-Δ V/f converter output clock

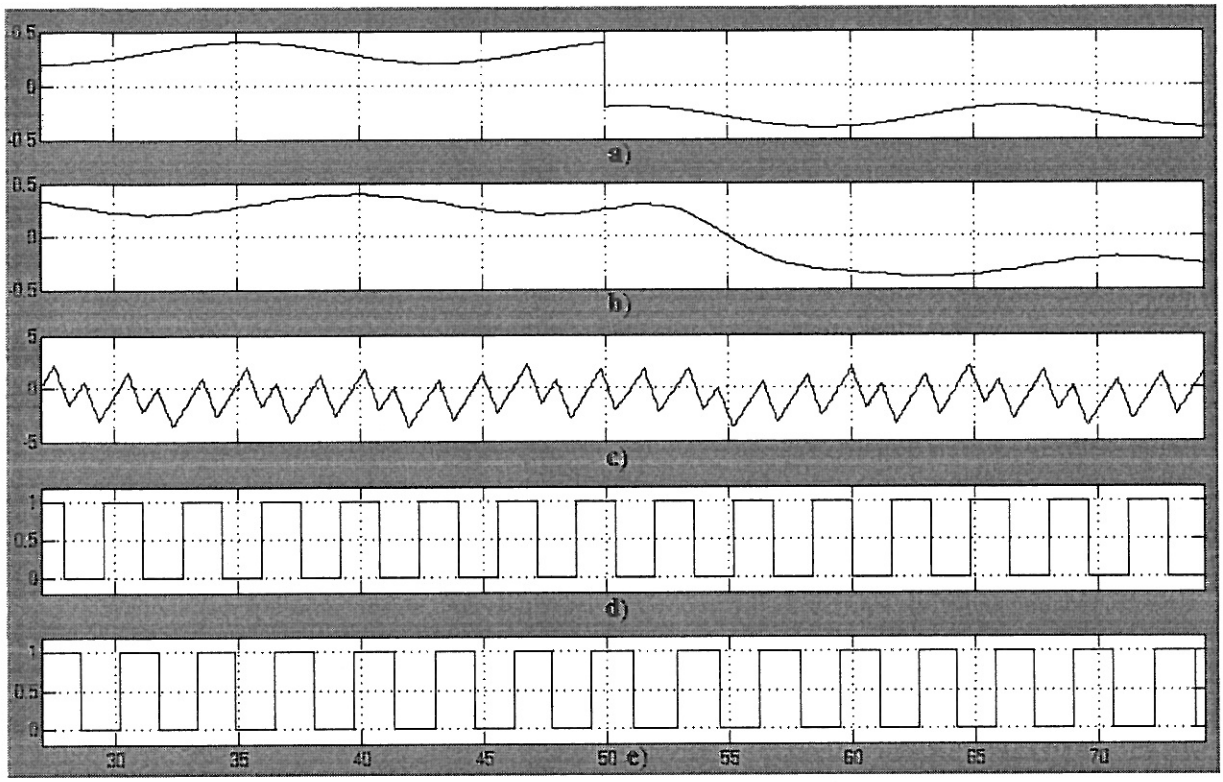


Figure 13. Time diagrams of: a) input voltage, b) output voltage, c) integrator output, d) Clk1clock, e) Σ-Δ V/f converter output clock